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Charissa D. Wheeler

APPLICATION FOR UNITED STATES LETTERS PATENT

S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that I, Ki-Min LEE, a citizen of Republic of Korea, residing at 891-10 Daechi-dong, Gangnam-gu, Seoul, Republic of Korea have invented a new and useful **METHODS OF MANUFACTURING METAL-INSULATOR-METAL CAPACITORS OF HIGH CAPACITANCE IN SEMICONDUCTOR DEVICES**, of which the following is a specification.

METHODS OF MANUFACTURING METAL-INSULATOR-METAL CAPACITORS OF HIGH CAPACITANCE IN SEMICONDUCTOR DEVICES

TECHNICAL FIELD

[0001] The present disclosure relates to semiconductors and, more particularly, to methods of manufacturing a metal-insulator-metal ("MIM") capacitors of high capacitance in semiconductor devices.

BACKGROUND

[0002] Referring to Fig. 1, generally, a conventional structure of an MIM capacitor includes an ARC (Antireflective Coated) TiN layer 20 deposited on a lower electrode (metal line) 10. An insulator layer 30 is deposited on the ARC TiN layer 20 and an upper electrode 40 is deposited on the insulator layer 30, sequentially.

[0003] In etching the insulator layer 30, however, the lower electrode (metal line) 10 is simultaneously etched, so that metallic polymers are sputtered on the surface of the lower electrode 10 and deposited on sidewalls of the insulator layer 30, thereby causing a short phenomenon. In addition, the upper electrode 40 and the lower electrode 10 are formed in a planar configuration. Accordingly, to form an MIM capacitor of high capacitance, a plan area of the electrodes should be increased.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Fig. 1 illustrates a cross sectional view of a conventional structure of an MIM capacitor in a semiconductor device.

[0005] Figs. 2A to 2F depict cross sectional views sequentially showing an example disclosed process of fabricating an MIM capacitor.

[0006] Figs. 3A to 3D offer cross sectional views sequentially showing a second example disclosed process of fabricating an MIM capacitor.

DETAILED DESCRIPTION

[0007] Figs. 2A to 2F depict cross sectional views sequentially showing an example disclosed process of fabricating an MIM capacitor. As shown in Fig. 2A, an interlayer dielectric film S20, which may be made of USG (Undoped Silicate Glass) or TEOS (Tetraethoxysilane) and into which an MIM capacitor is to be formed, is deposited on a metal line S10. By controlling the thickness of the interlayer dielectric film S20, an MIM capacitor of desired capacitance may be fabricated.

[0008] Subsequently, referring to Fig. 2B, a photoresist pattern S30 is formed on the interlayer dielectric film S20, and as shown in Fig. 2C, the interlayer dielectric film S20 is etched to form an MIM capacitor forming region S40. The photoresist pattern S30 is then removed.

[0009] As shown in Fig. 2D, a lower electrode layer S50, an insulator layer S60 and an upper electrode layer S70 are sequentially deposited on the interlayer dielectric film S60 having the MIM capacitor forming region S40.

[0010] At this time, the lower electrode layer S50 may be made of Ti, W, TiN or the like; the insulator layer S60 is made of TaO_2, Al_2O_3, SiN or the like; the upper electrode layer S70 is made of Ru, Pt, TiN or the like.

[0011] Thereafter, a photoresist pattern S80 is formed on the upper electrode layer S70 as shown in Fig. 2E and an MIM capacitor as shown in Fig. 2F is formed by etching the lower electrode layer S50, the insulator layer S60 and the upper electrode layer S70 using the photoresist pattern S80 as a mask.

[0012] Figs. 3A to 3D offer cross sectional views sequentially showing a second example disclosed process of fabricating an MIM capacitor. As shown in Fig. 3A, an interlayer dielectric film SS20 into which an MIM capacitor is to be formed is deposited on a metal line SS10. By controlling the thickness of the interlayer dielectric film SS20, an MIM capacitor of desired capacitance may be obtained. The interlayer dielectric film SS20 is then planarized by a CMP process or an etch-back process, and a photoresist pattern SS30 is formed thereon. Subsequently, as shown

in Fig. 3B, the interlayer dielectric film SS20 is etched by using the photoresist pattern SS30 as a mask to form an MIM capacitor forming region SS80.

[0013] As shown in Fig. 3C, a lower electrode layer SS40, an insulator layer SS50 and an upper electrode layer SS60 are sequentially deposited on the interlayer dielectric film SS50 having the MIM capacitor forming region SS80.

[0014] According to one example, the lower electrode layer SS40 may be made of Ti, W, TiN or the like; the insulator layer SS50 may be made of TaO_2, Al_2O_3, SiN or the like; the upper electrode layer SS60 may be made of Ru, Pt, TiN or the like.

[0015] Finally, as shown in Fig. 3D, the lower electrode SS40, the insulator layer SS50 and the upper electrode SS60 are planarized to expose the interlayer dielectric film SS30 by a CMP process or an etch-back process.

According to the disclosed example processes, the MIM capacitor has an increased capacitance in proportion to the thickness of the interlayer dielectric film without increasing a plan area of the electrodes, thereby facilitating a high integration of the semiconductor device. Further, a short phenomenon, which may be caused by metallic polymers in a conventional process, is prevented.

[0016] According to a first example, a method for fabricating an MIM capacitor of high capacitance in a semiconductor device includes depositing an interlayer

dielectric film on a metal line; etching the interlayer dielectric film to form an MIM capacitor forming region; sequentially depositing a lower electrode, an insulator layer and an upper electrode on the interlayer dielectric film; and etching the lower electrode, the insulator layer and the upper electrode to form an MIM capacitor.

[0017] According to a second disclosed example, a method of fabricating an MIM capacitor of high capacitance in a semiconductor device includes depositing an interlayer dielectric film on a metal line; planarizing the interlayer dielectric film; etching the interlayer dielectric film to form an MIM capacitor forming region; sequentially depositing a lower electrode, an insulator layer and an upper electrode on the interlayer dielectric film; and planarizing the lower electrode, the insulator layer and the upper electrode to form an MIM capacitor.

[0018] Although certain example methods are disclosed herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers every apparatus, method and article of manufacture fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.